

WE CLAIM AS OUR INVENTION:

1. A method for operating a mail-processing device having at least one printhead comprising the steps of:

storing binary pixel data, representing information to be printed by said at least one printhead, stored as a plurality of data strings in a pixel memory in the form of data words, with a predefined number of successive data words forming each data string;

providing a print data controller having access to said pixel memory and connecting said print data controller to said at least one printhead for controlling printing of said information by said at least one printhead, and including in said print data controller a DMA controller and an address generator and, for each printhead, a print data editing unit, the print data editing unit containing two buffer memories; and

via said DMA controller, transferring said binary pixel data word-by-word from said pixel memory into said two buffer memories and entering successive words of one of said data strings being alternately into one of said two buffer memories, for intermediate storage therein editing the data words stored in the other of the two buffer memories, at respective addresses designated by said address generator, and printing said edited information represented by the data words.

2. A method as claimed in claim 1 comprising generating address signals and control signals relating to said intermediate storage of said data words in said two buffer memories using said DMA-controller, editing said data words using said address generator, for supplying said address signals and said control signals to said pixel data editing unit, and transferring said data words respectively stored in

said buffer memories for editing into said pixel data editing unit in selected groups and in a selected sequence dependent on said address signals and said control signals.

3. A method as claimed in claim 1 comprising generating address write signals in said DMA controller and using said address write signals to write said data words of said data string from said pixel memory respectively into said two buffer memories, and counting said predetermined number of data words with a cycle counter in said DMA controller.

4. A method as claimed in claim 1 comprising generating, in said printer controller, a switchover signal, supplied to said pixel data editing unit for controlling transfer of the respective data words, for editing by said pixel data editing unit, to said at least one printhead for printing said information, and also supplying said switchover signal to said DMA controller and generating respective selection signals in said DMA controller, dependent on said switchover signal.

5. A method as claimed in claim 1 wherein said mail-processing device comprises first and second printheads, and wherein said print data controller comprises a first print data editing unit having two buffer memories and a second print data editing unit having two buffer memories, and wherein said DMA controller includes a cycle counter, and comprising the steps of generating a switchover signal in said print data controller and supplying said switchover signal to said DMA controller, and generating a DMA start signal in said DMA controller which causes said cycle counter to begin counting a predetermined number of data words in said data string from said pixel memory, and dependent on said switchover signal, supplying a respective selection signal from said DMA controller to said first pixel data editing unit until said predetermined number of data words is reached, and said

DMA controller to supplying a respective selection signal to said second pixel data editing unit after said predetermined number of data words is reached, and generating a DMA busy signal having a zero value after a second predetermined number of data words is counted by said cycle counter, to end counting by said cycle counter.

6. A method as claimed in claim 5 comprising providing, each of said first and second pixel data editing units, a shift register operable in combination with the two buffer memories in that pixel editing unit, for parallel-to-serial conversion of said pixel data and comprising generating a load signal in said address generator and supplying said load signal to the shift register in each of said first and second print data editing units to cause loading of serial data from the respective print registers to the respective first and second printheads.

7. A method as claimed in claim 6 comprising generating an address read signal having a plurality of bits in said address generator, including more significant bits which designate an address in the first and second buffer memories, and less significant bits which allow addressing within a data word.

8. A method as claimed in claim 1 comprising conveying items past said at least one printhead on which said information is to be printed by said at least one printhead, and generating encoder signals indicating a position of an item relative to said at least one printhead, and supplying said encoder signal to said printer controller, wherein said printer controller comprises a data string counter and incrementing said data string counter after each data string is printed, and ending printing of said information when said data string counter reaches a predetermined count.

9. A method as claimed in claim 1 wherein said DMA controller comprises a cycle counter for counting said data words, generating a DMA start signal and supplying said DMA start signal to said DMA controller, and starting said cycle counter upon receipt of said DMA start signal, and subsequently generating a DMA busy signal having a value zero if the period of time with a number of DMA cycles has ended.

10. A method as claimed in claim 1 comprising employing a dual port RAM as each of said buffer memories.

11. A method as claimed in claim 10 wherein said print data controller comprises a first multiplexer having inputs connected to a first of said dual port RAMs, a second multiplexer having inputs connected to a second of said dual port RAMs, a third multiplexer having inputs connected to respective outputs of said first and second multiplexers, a demultiplexer having an input connected to an output of said third multiplexer and a collecting register having inputs connected to outputs of said demultiplexer and comprising the steps of, in said first multiplexer, selecting a single bit of said pixel data from said first of said dual port RAMs when less-significant bits of an address read signal, generated by said address generator, is supplied thereto, and in second multiplexer selecting a single bit of pixel data from said second of said dual port RAMs, and via said third multiplexer, dependent on a switchover signal generated by said print data controller, transferring the respective bits from said first and second multiplexers to said demultiplexer, and from said demultiplexer transferring successive single bits into said collecting register at respective addresses determined by an address signal supplied to said demultiplexer.

12. A method as claimed in claim 11 further comprising connecting shift register to said collecting register for transferring said bits from said collecting register to said at least one printhead.

13. A method as claimed in claim 1 comprising employing an application-specific integrated circuit as said print data controller.

14. A method as claimed in claim 1 comprising employing a programmable logic chip as said print data controller.